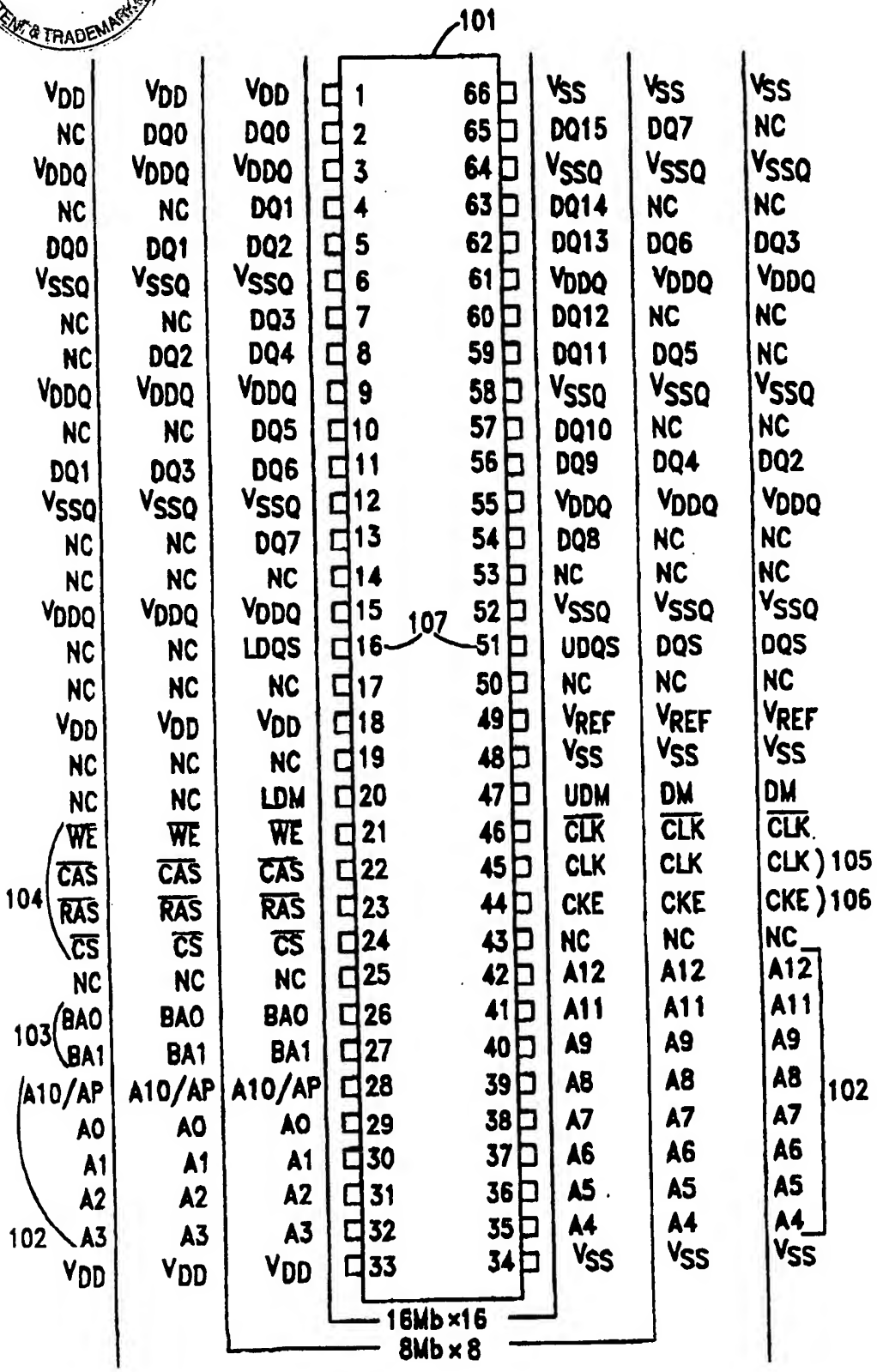
10/072,346

FIG. 1



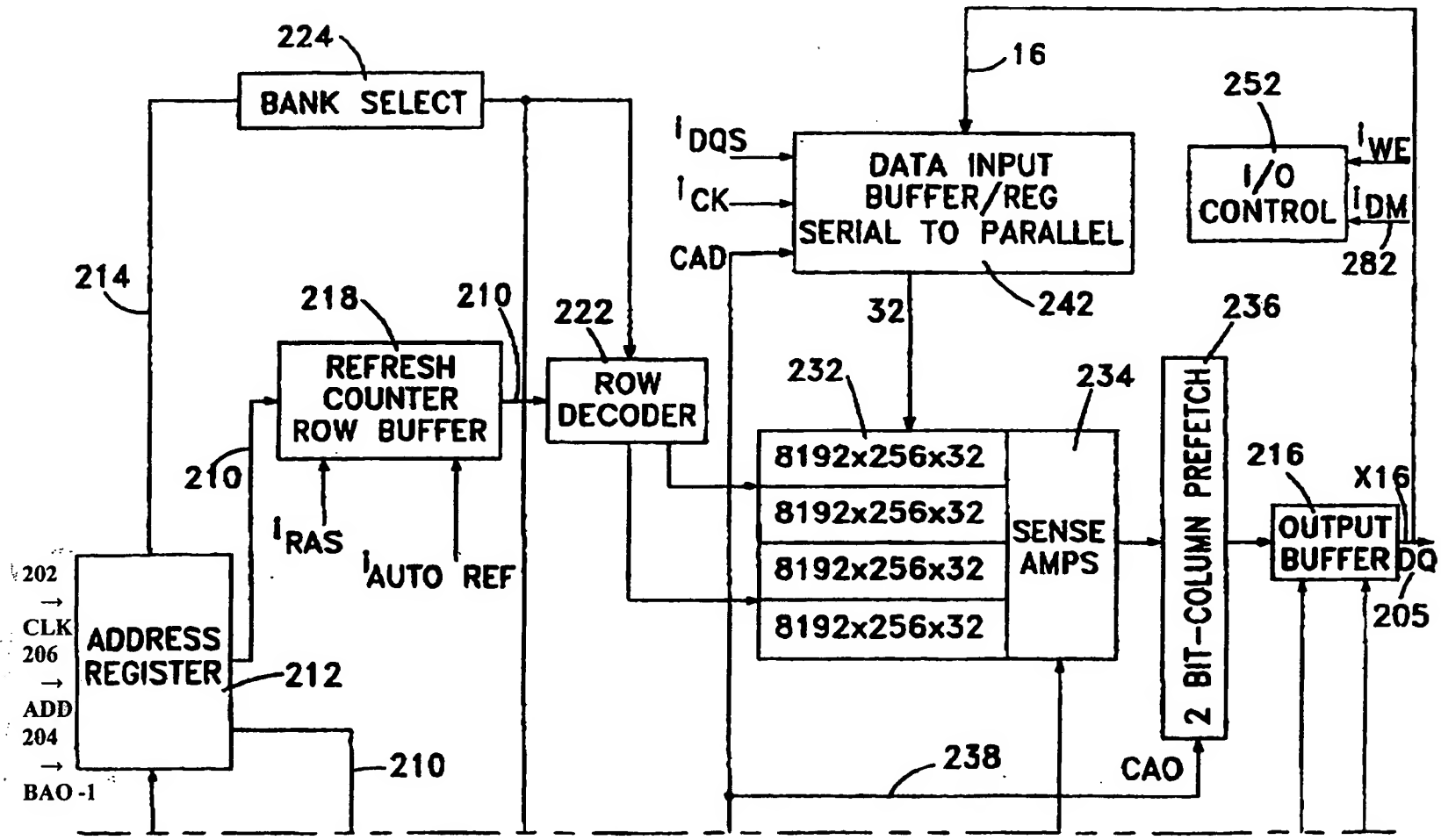

224
BANK SELECT
16
252
DQS
CK
CAD
DATA INPUT
BUFFER/REG
SERIAL TO PARALLEL
I/O
CONTROL
WE
DM
282
214
218
210
222
32
242
236
REFRESH
COUNTER
ROW BUFFER
ROW
DECODER
232
234
210
8192x256x32
8192x256x32
8192x256x32
8192x256x32
SENSE
AMPS
2 BIT-COLUMN PREFETCH
216
X16
OUTPUT
BUFFER
DQ
205
RAS
AUTO REF
202
CLK
206
ADD
204
BAO-1
ADDRESS
REGISTER
212
210
238
CAO

FIG. 2A

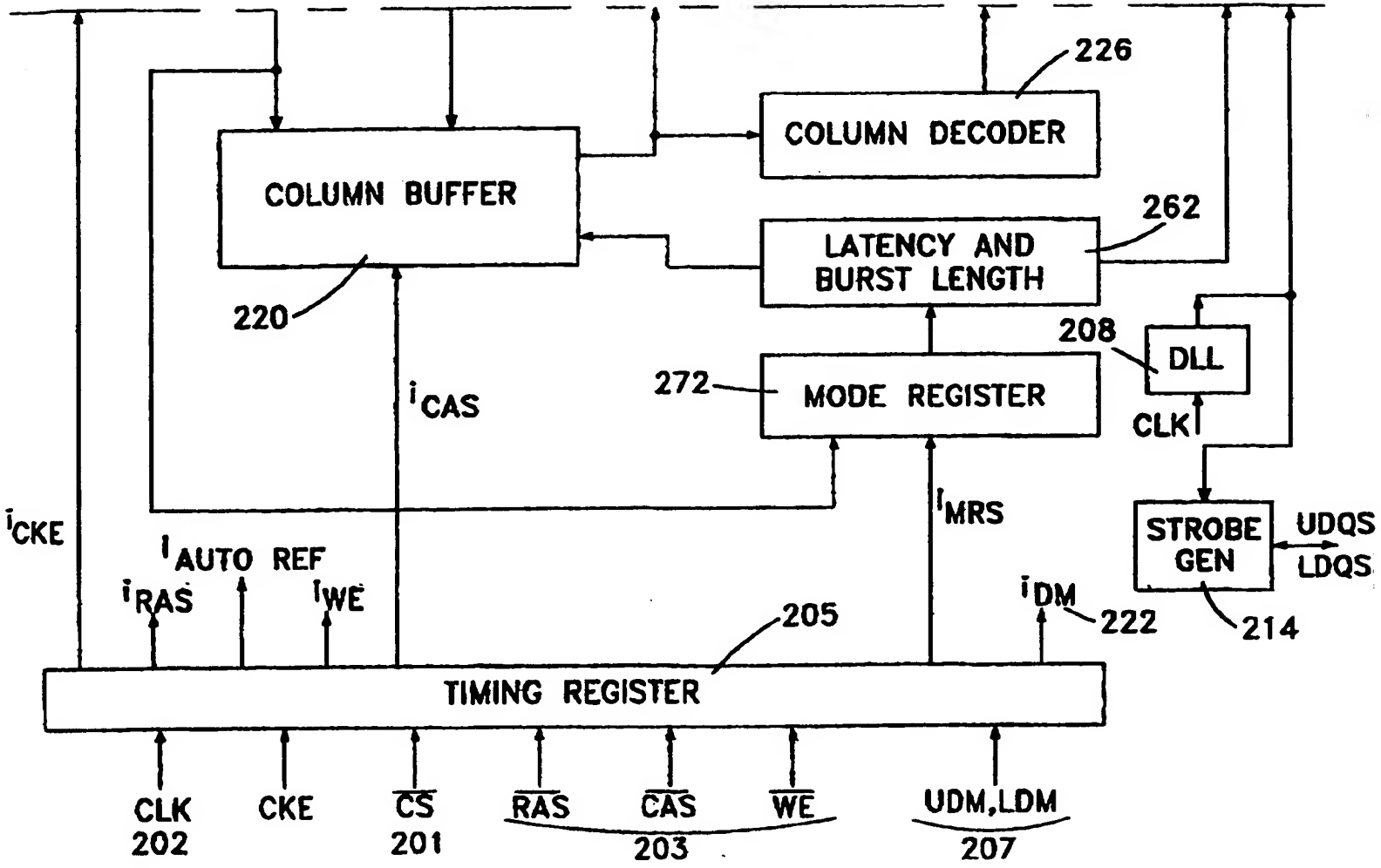

226
COLUMN DECODER
COLUMN BUFFER
262
LATENCY AND BURST LENGTH
220
208
DLL
272
MODE REGISTER
CLK
i_{CAS}
i_{CKE}
$i_{AUTO\ REF}$
i_{RAS}
i_{WE}
i_{MRS}
STROBE GEN
UDQS
LDQS
i_{DM}
222
214
205
TIMING REGISTER
CLK
202
CKE
CS
201
RAS
CAS
WE
203
UDM,LDM
207

FIG. 2 B

Operation	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DM	BA_0, BA_1	A_{10}	A_0~A_9, A_{11}	MNE	Notes
	n-1	n										
Device Deselect	H	X	H	X	X	X	X	X	X	X	INHBT	
No Operation	H	X	L	H	H	H	X	X	X	X	NOP	
Load Mode Register Mode or Extended Mode Register	H	X	L	L	L	L	X	OP CODE			MRS/EMRS	1
Row Activate	H	X	L	L	H	H	X	BS	Row Address		ACT	2
Read	H	X	L	H	L	H	X	BS	L	Col.	RD	3
Read w/ Auto Precharge	H	X	L	H	L	H	X	BS	H	Col.	RAP	3
Write	H	X	L	H	L	L	V	BS	L	Col.	WR	3, 4
Write w/ Auto Precharge	H	X	L	H	L	L	V	BS	H	Col.	WAP	3, 4
Burst Stop	H	X	L	H	H	L	X	X	X	X	BST	5
Precharge Single Bank	H	X	L	L	H	L	X	BS	L	X	PRE	
Precharge All Banks	H	X	L	L	H	L	X	X	H	X	PREALL	
Auto Refresh	H	H	L	L	L	H	X	X	X	X	REF	1
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X	SR(ENTRY)	1
Self Refresh Exit	L	H	H	X	X	X	X	X	X	X	SR(EXIT)	
	L	H	L	H	H	H	X	X	X	X		
Power Down Mode (Entry)	H	L	H	X	X	X	X	X	X	X	PDN(ENTRY)	
	H	L	L	H	H	H	X	X	X	X		
Power Down Mode (Exit)	L	H	X	X	X	X	X	X	X	X	PDN(EXIT)	

1. Should be issued only after both banks are deactivated (PREALL command).
2. Should be issued only after the corresponding bank has been deactivated (PRE command).
3. Should be issued after the corresponding bank has been activated (ACT command).
4. Any valid Write cycles applied to the selected bank/row will be masked according to the DM.
5. Should be issued only during read burst cycles.

FIG. 3

FIG. 4A

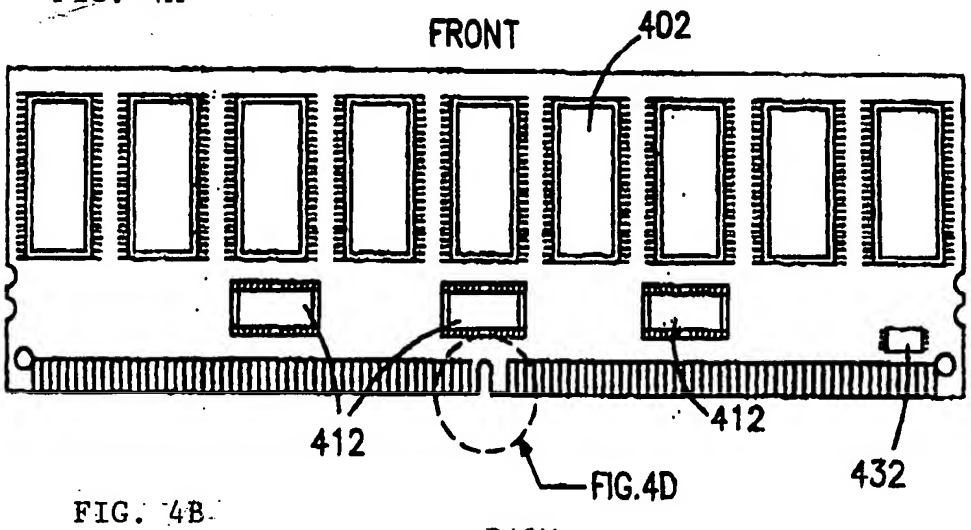
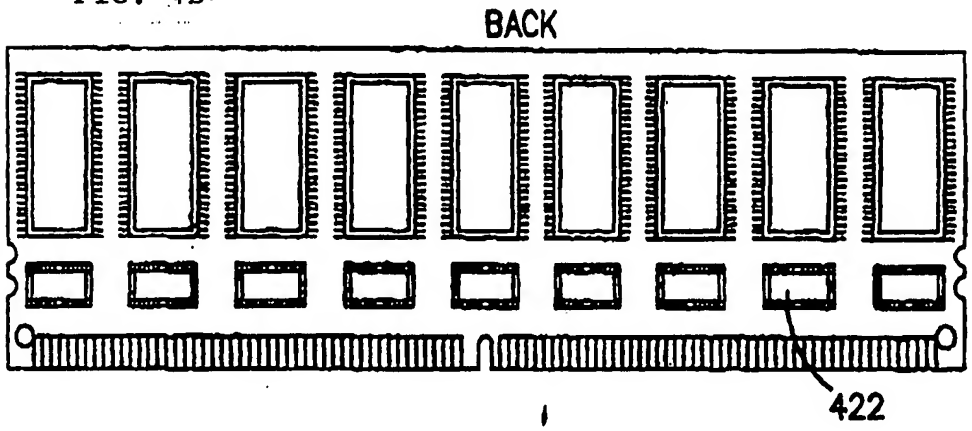


FIG. 4B



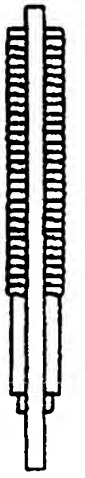


FIG. 4C

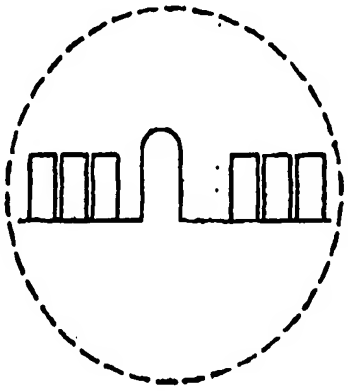


FIG. 4D

FIG. 5A

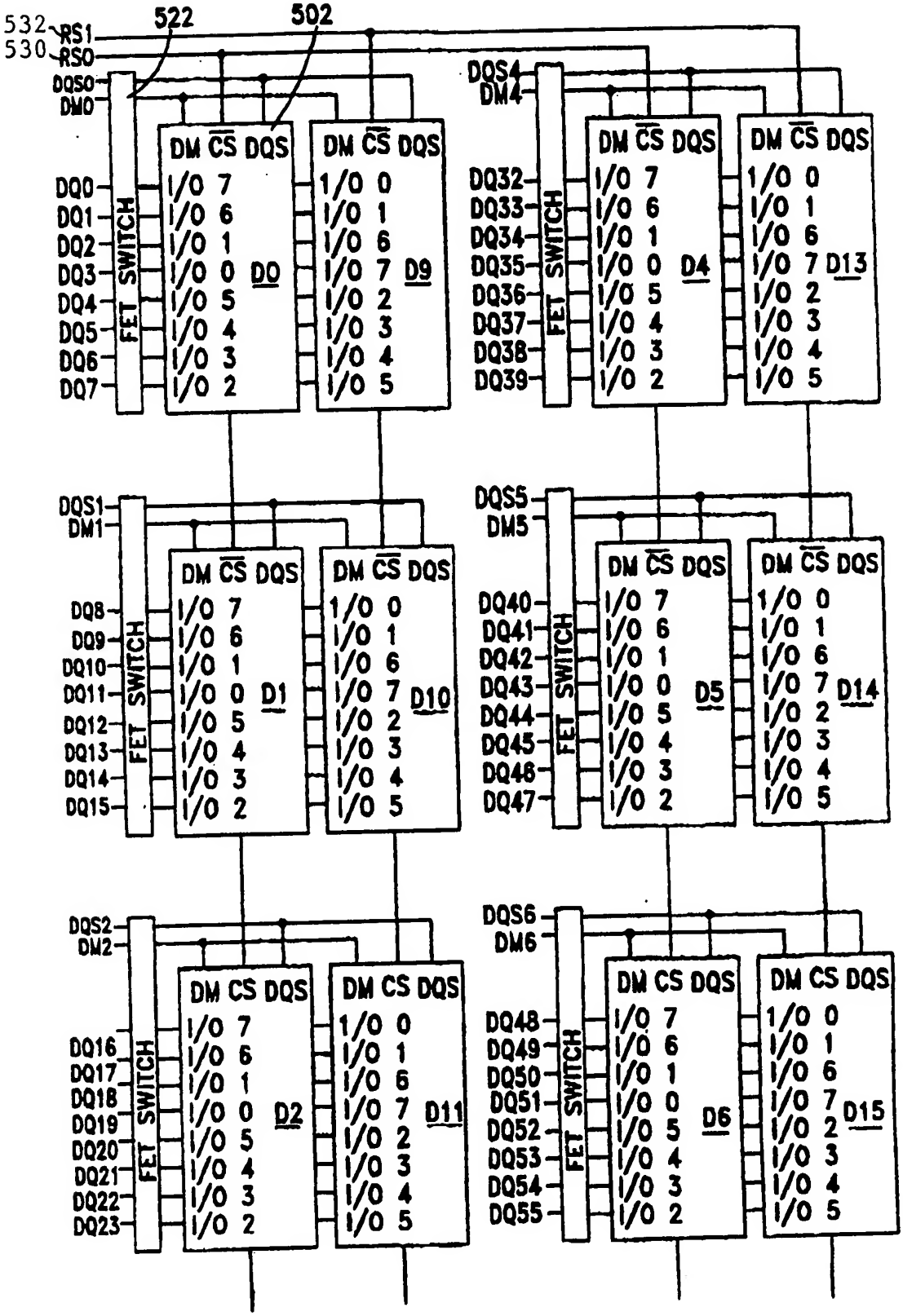

532
530
RS1
RS0
522
502
DQS0
DM0
DQS4
DM4
DQS1
DM1
DQS5
DM5
DQS2
DM2
DQS6
DM6
FET SWITCH
DM CS DQS
I/O 7
I/O 6
I/O 1
I/O 0
I/O 5
I/O 4
I/O 3
I/O 2
I/O 0
I/O 1
I/O 6
I/O 7
I/O 2
I/O 3
I/O 4
I/O 5
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
D0
D9
DQ32
DQ33
DQ34
DQ35
DQ36
DQ37
DQ38
DQ39
D4
D13
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
D1
D10
DQ40
DQ41
DQ42
DQ43
DQ44
DQ45
DQ46
DQ47
D5
D14
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
D2
D11
DQ48
DQ49
DQ50
DQ51
DQ52
DQ53
DQ54
DQ55
D6
D15

FIG. 5B

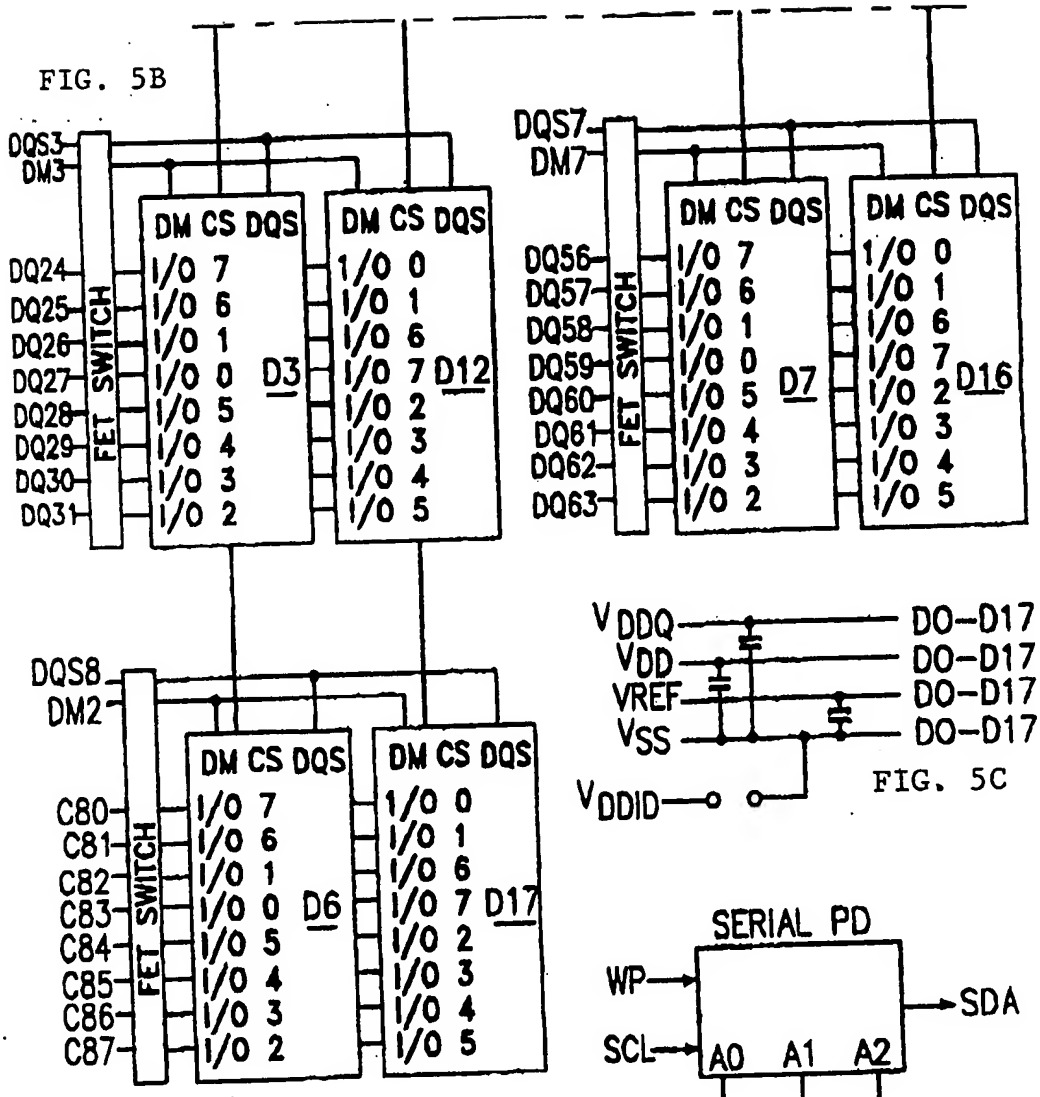


FIG. 5C

FIG. 5E

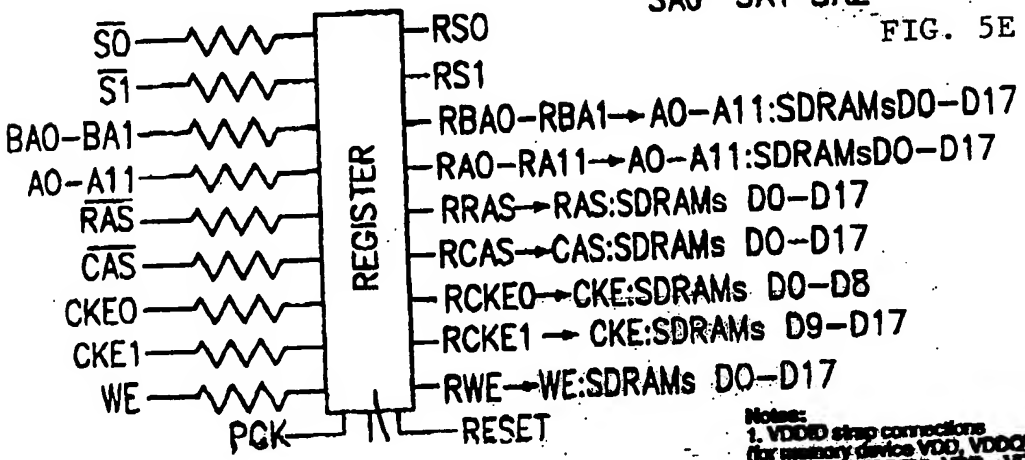


FIG. 5D

Notes:
1. VDDID strap connections
(for memory device VDD, VDDQ):
STRAP OUT (OPEN): VDD ≠ VDDQ
STRAP IN (VSS): VDD = VDDQ
2. See FET switch detail for more information.

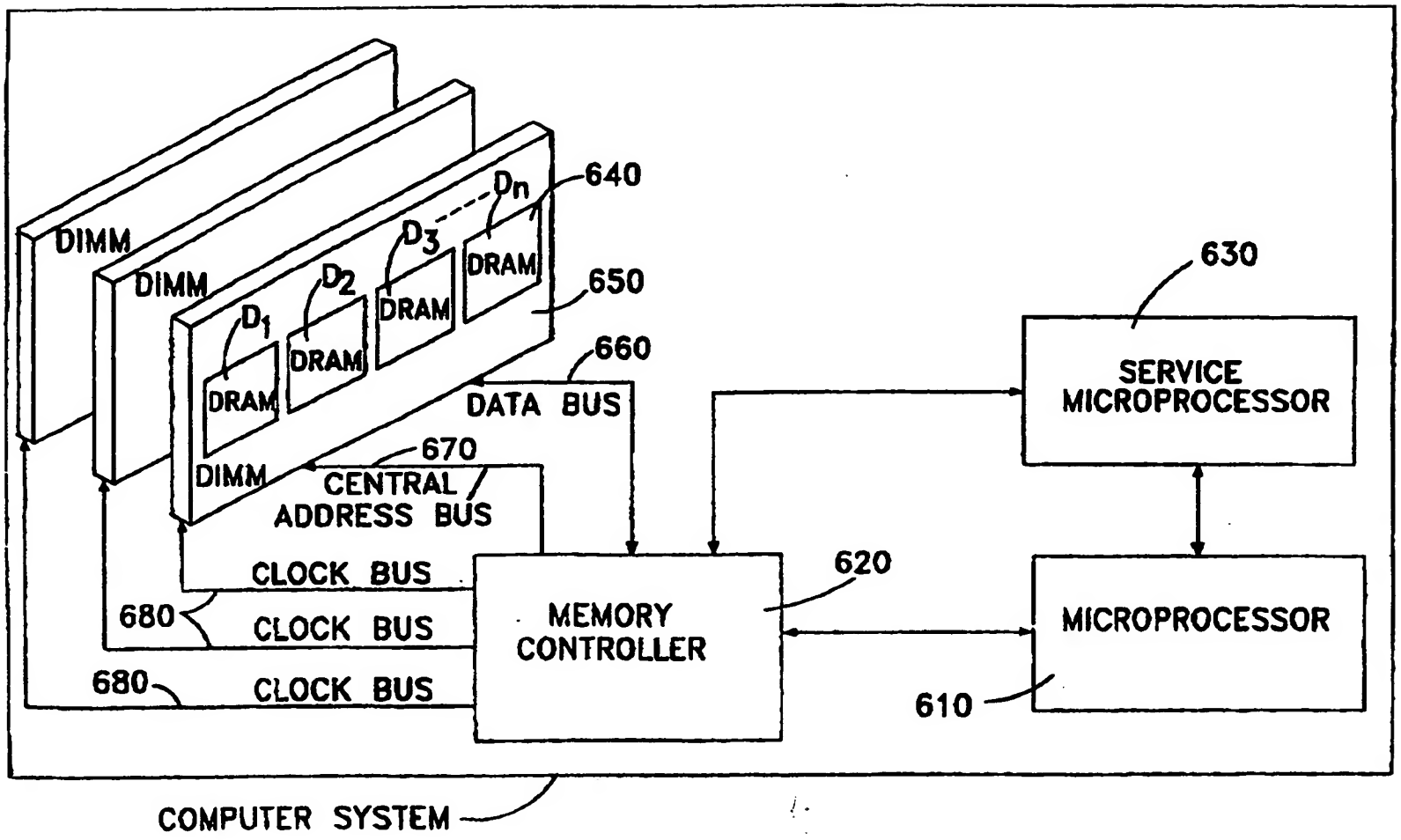

DIMM
DIMM
DIMM
DRAM
DRAM
DRAM
DRAM
D1
D2
D3
Dn
640
650
660
DATA BUS
670
CENTRAL
ADDRESS BUS
CLOCK BUS
680
CLOCK BUS
680
CLOCK BUS
MEMORY
CONTROLLER
620
630
SERVICE
MICROPROCESSOR
MICROPROCESSOR
610
COMPUTER SYSTEM

FIG. 6

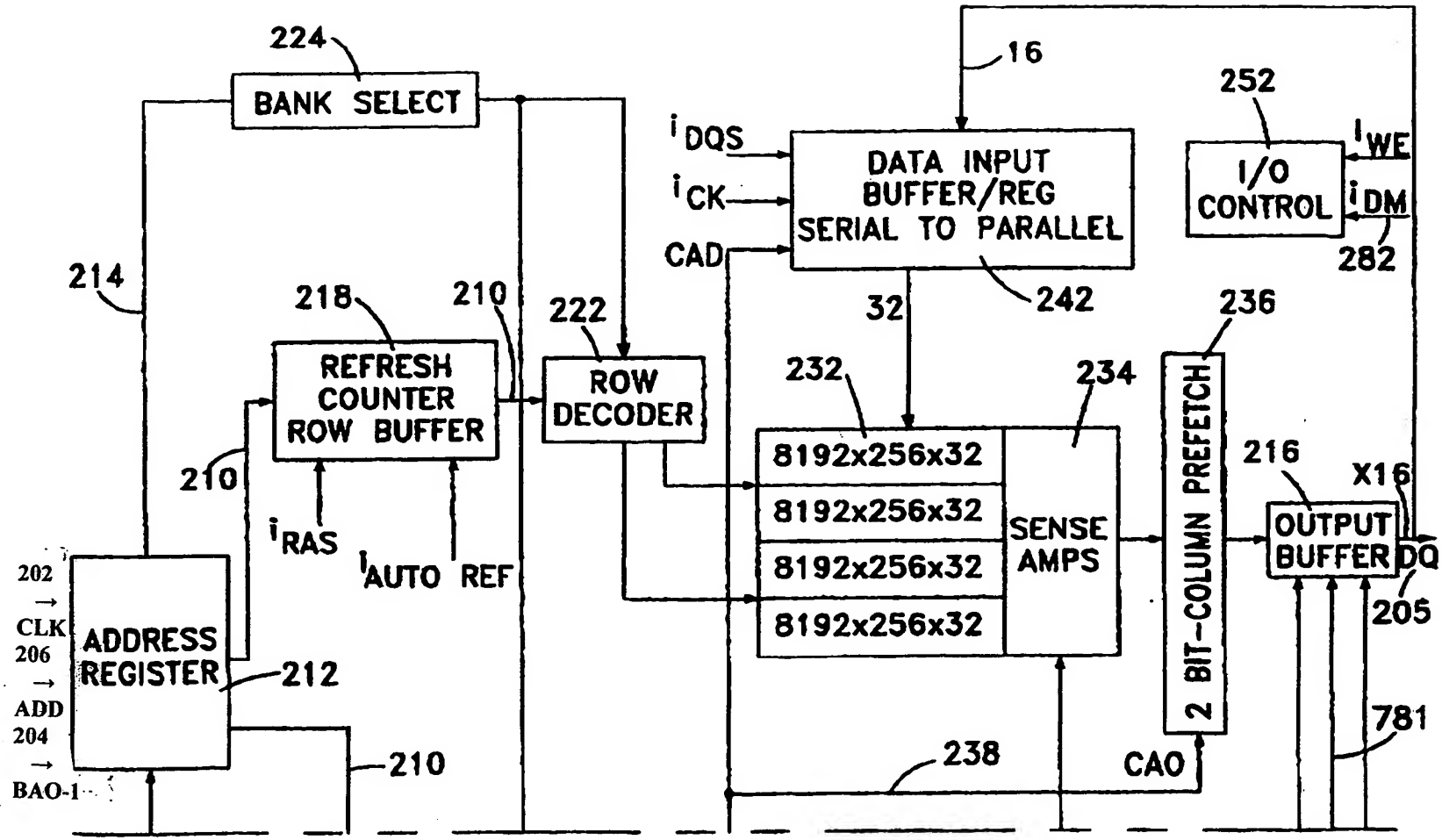

224
BANK SELECT
16
252
I/O CONTROL
iWE
iDM
282
iDQS
iCK
CAD
DATA INPUT BUFFER/REG SERIAL TO PARALLEL
242
32
214
218
210
222
REFRESH COUNTER ROW BUFFER
ROW DECODER
232
234
236
8192x256x32
8192x256x32
8192x256x32
8192x256x32
SENSE AMPS
2 BIT-COLUMN PREFETCH
216
X16
OUTPUT BUFFER
DQ
205
781
210
iRAS
iAUTO REF
202
CLK
206
ADD
204
BAO-1
ADDRESS REGISTER
212
210
238
CAO

FIG. 7A

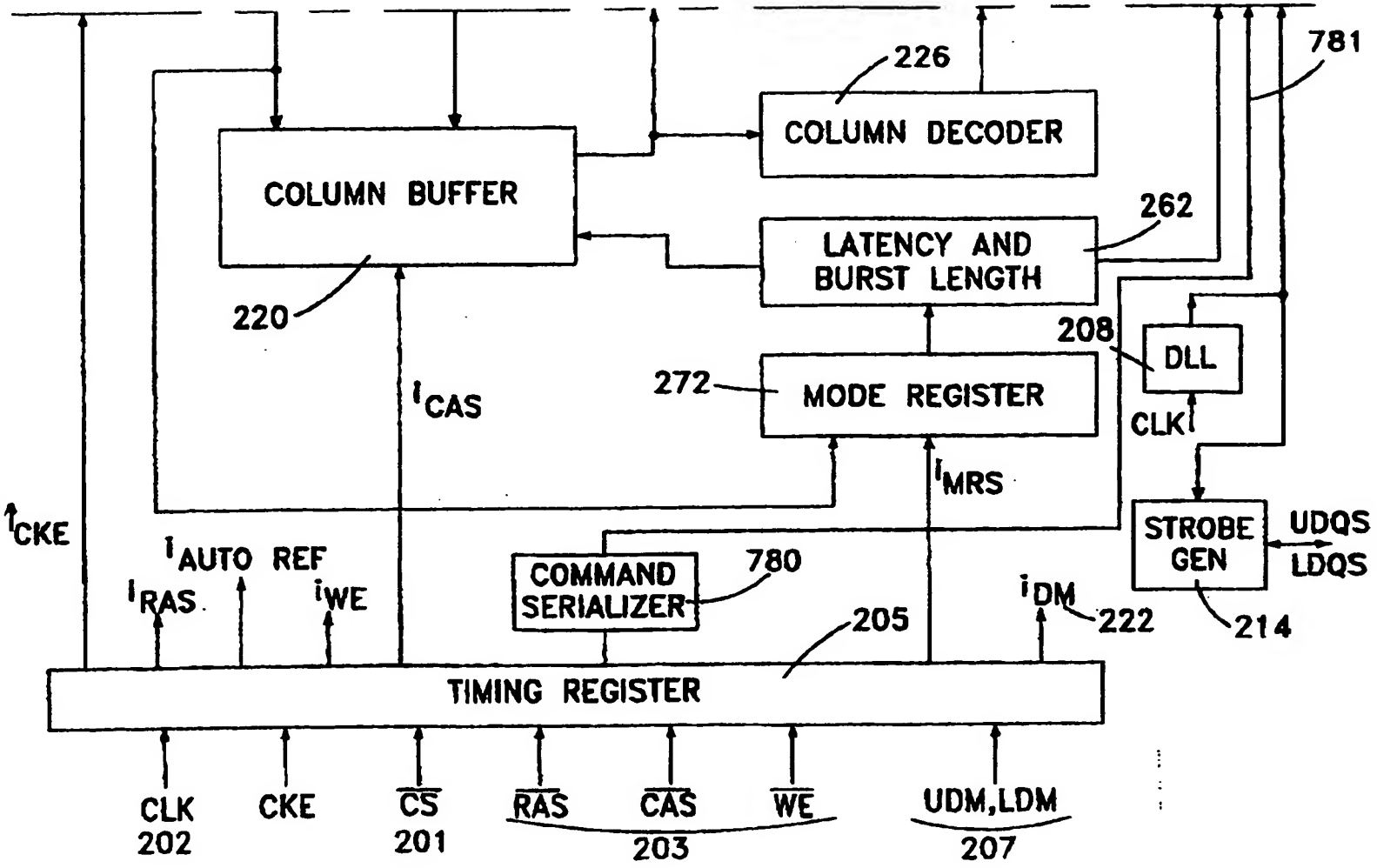

781
226
COLUMN DECODER
COLUMN BUFFER
262
LATENCY AND BURST LENGTH
220
208
DLL
272
MODE REGISTER
CLK
ICAS
IMRS
ICKE
STROBE GEN
UDQS
LDQS
IAUTO REF
IRAS
IWE
COMMAND SERIALIZER
780
IDM
222
214
205
TIMING REGISTER
CLK 202
CKE
CS 201
RAS
CAS
WE
203
UDM,LDM 207

FIG. 7B

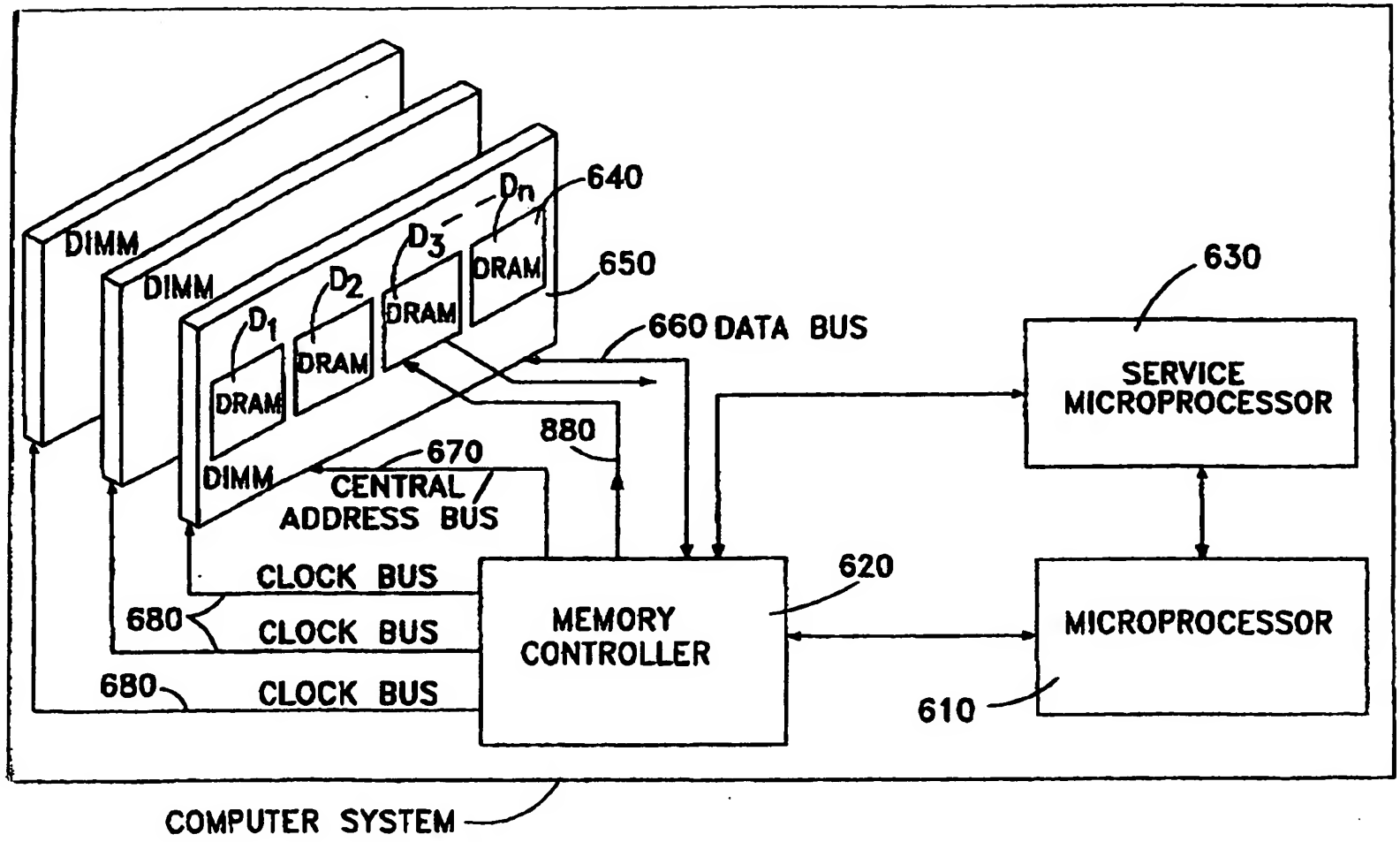

DIMM
DIMM
DIMM
DRAM
DRAM
DRAM
DRAM
D1
D2
D3
Dn
640
650
630
660 DATA BUS
SERVICE MICROPROCESSOR
880
670
CENTRAL ADDRESS BUS
CLOCK BUS
CLOCK BUS
CLOCK BUS
680
680
620
MEMORY CONTROLLER
MICROPROCESSOR
610
COMPUTER SYSTEM

FIG. 8

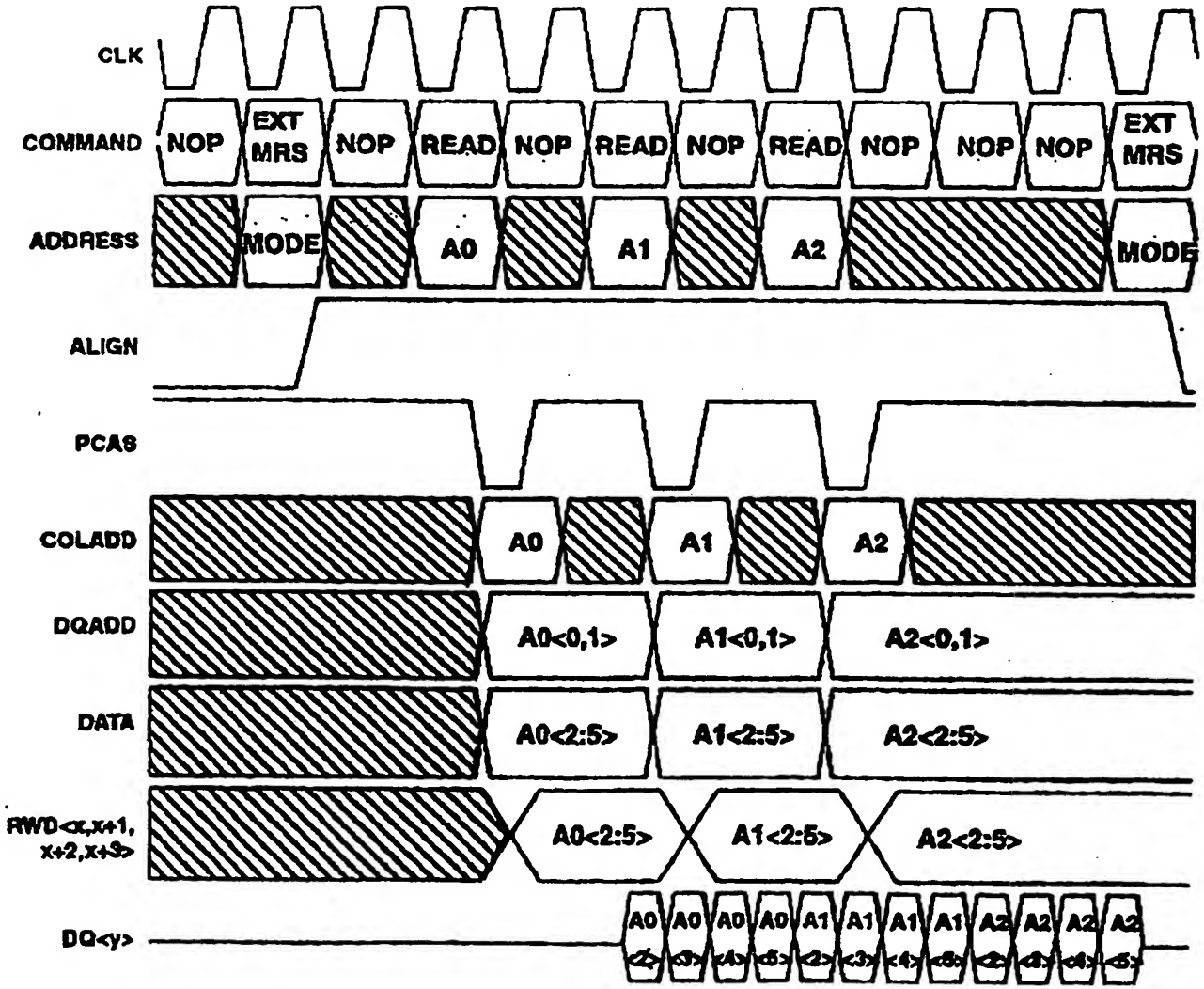

CLK
COMMAND
NOP
EXT MRS
NOP
READ
NOP
READ
NOP
READ
NOP
NOP
NOP
EXT MRS
ADDRESS
MODE
A0
A1
A2
MODE
ALIGN
PCAS
COLADD
A0
A1
A2
DQADD
A0<0,1>
A1<0,1>
A2<0,1>
DATA
A0<2:5>
A1<2:5>
A2<2:5>
RWD<x,x+1, x+2,x+3>
A0<2:5>
A1<2:5>
A2<2:5>
DQ<y>
A0 A0 A0 A0 A1 A1 A1 A1 A2 A2 A2 A2

FIG. 9

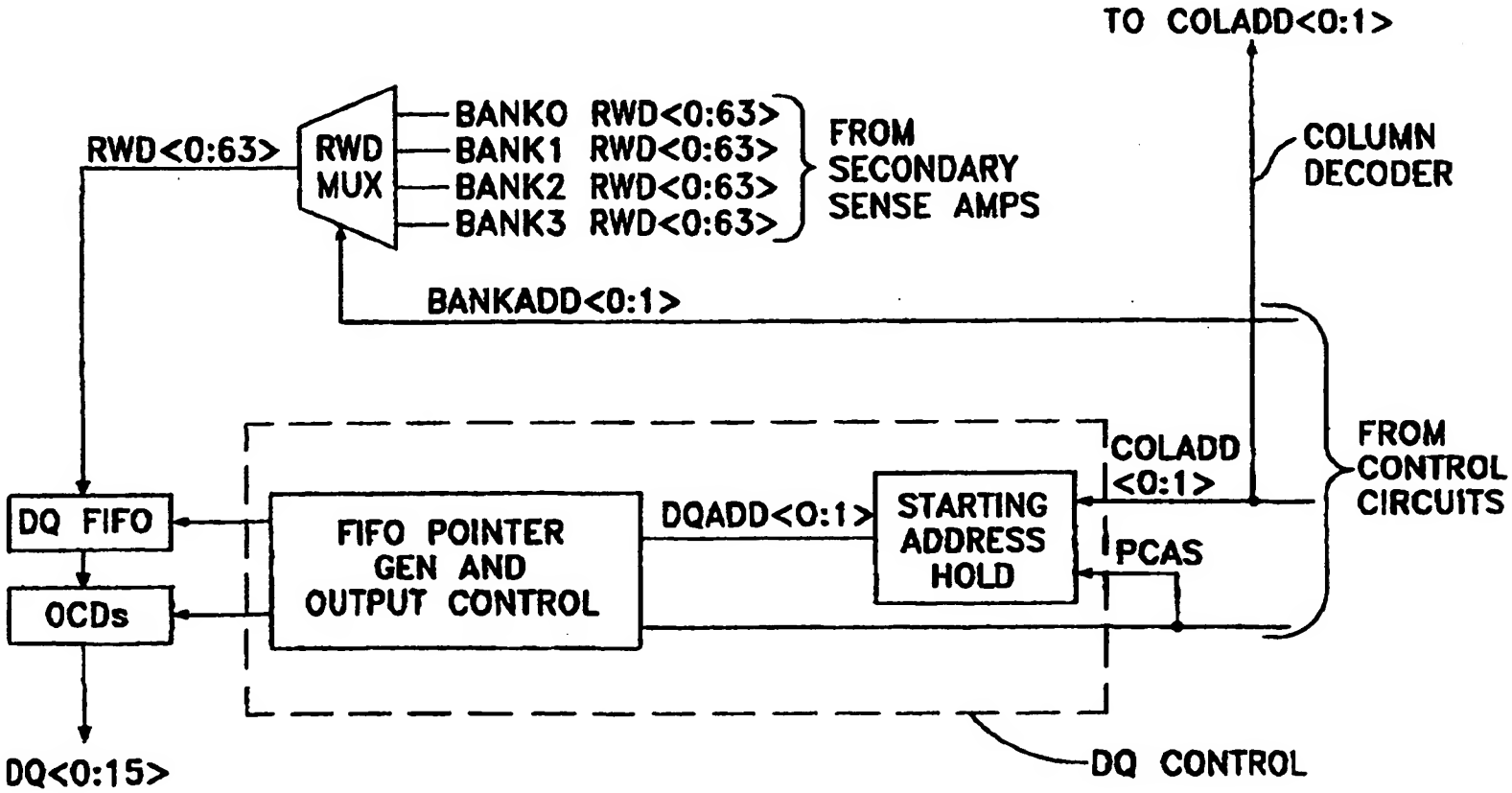

TO COLADD<0:1>
COLUMN DECODER
RWD<0:63>
RWD MUX
BANK0 RWD<0:63>
BANK1 RWD<0:63>
BANK2 RWD<0:63>
BANK3 RWD<0:63>
FROM SECONDARY SENSE AMPS
BANKADD<0:1>
FROM CONTROL CIRCUITS
COLADD <0:1>
DQ FIFO
FIFO POINTER GEN AND OUTPUT CONTROL
DQADD<0:1>
STARTING ADDRESS HOLD
PCAS
OCDs
DQ<0:15>
DQ CONTROL

FIG. 10

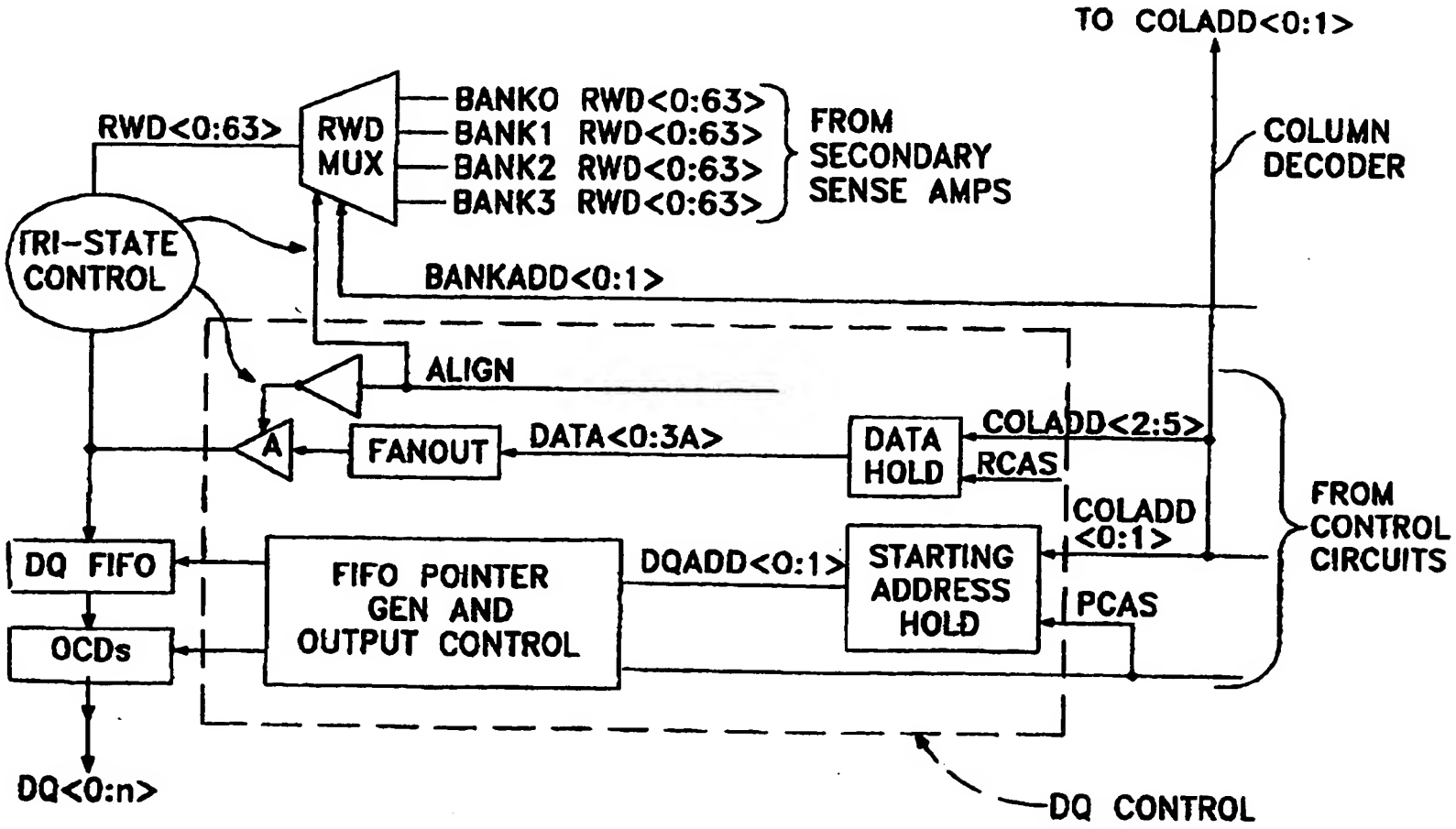

TO COLADD<0:1>
COLUMN DECODER
RWD<0:63>
RWD MUX
BANK0 RWD<0:63>
BANK1 RWD<0:63>
BANK2 RWD<0:63>
BANK3 RWD<0:63>
FROM SECONDARY SENSE AMPS
TRI-STATE CONTROL
BANKADD<0:1>
ALIGN
A
FANOUT
DATA<0:3A>
DATA HOLD
COLADD<2:5>
RCAS
COLADD <0:1>
FROM CONTROL CIRCUITS
DQ FIFO
FIFO POINTER GEN AND OUTPUT CONTROL
DQADD<0:1>
STARTING ADDRESS HOLD
PCAS
OCDs
DQ<0:n>
DQ CONTROL

FIG. 11

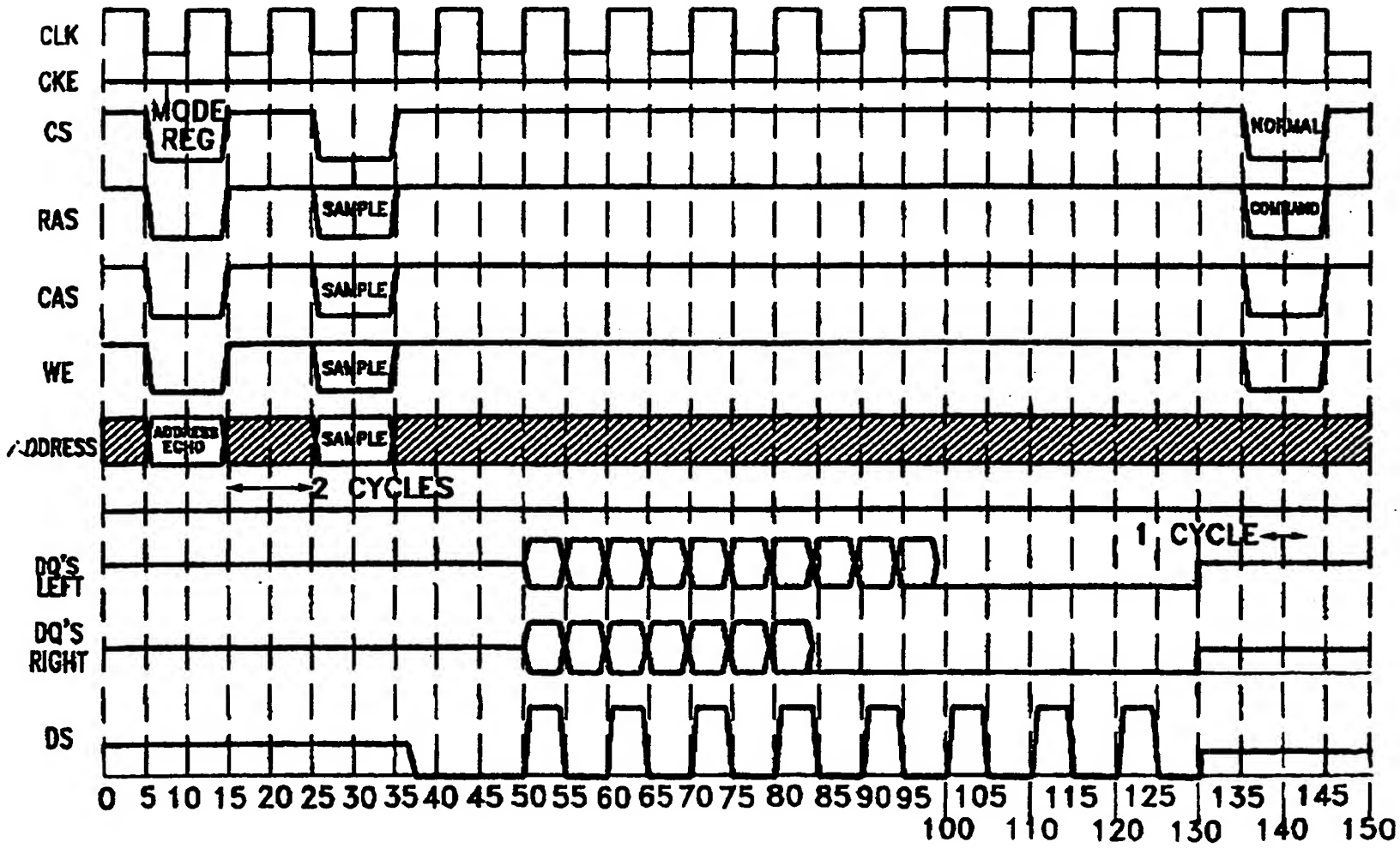

CLK
CKE
CS
RAS
CAS
WE
ADDRESS
DQ'S LEFT
DQ'S RIGHT
DS
MODE REG
NORMAL
SAMPLE
COMMAND
ADDRESS ECHO
2 CYCLES
1 CYCLE
0 5 10 15 20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95 100 105 110 115 120 125 130 135 140 145 150

FIG. 12